What is claimed is:

1. A method for forming a multilayer circuit substrate, comprising:

providing a dielectric base substrate;

forming conductors on the base substrate;

forming sacrificial structures on the base substrate and conductors to define areas to be protected from deposition of a dielectric layer;

vacuum depositing a dielectric thin film on the base substrate, the conductors and the sacrificial structures; and

removing the sacrificial structures to leave a patterned deposited dielectric thin film on the conductors and the base substrate.

2. The method claimed in claim 1, wherein forming the conductors comprises:

depositing a blanket layer of a conductor material; and

patterning the blanket layer of conductor material.

3. The method claimed in claim 2, wherein the blanket layer of conductor material is formed by physical vapor deposition.

4. The method claimed in claim 2, wherein the blanket layer of conductor material is formed by evaporation.

5. The method claimed in claim 2, wherein the blanket layer of conductor material is formed by chemical vapor deposition.

6. The method claimed in claim 2, wherein the blanket layer of conductor material is patterned by a photoresist lift-off process.

7. The method claimed in claim 2, wherein the blanket layer of conductor material is patterned by a chemical etching process.

8. The method claimed in claim 1, wherein the conductors are formed by a shadow mask patterning process.

9. The method claimed in claim 1, wherein the conductors are formed by a screen printing process.

10. The method claimed in claim 1, wherein the sacrificial structures are formed by a shadow mask deposition process.

11. The method claimed in claim 10, wherein the sacrificial structures are formed of aluminum and are removed using a ferric chloride solution.

12. The method claimed in claim 10, wherein the shadow mask deposition process utilizes a shadow mask having laser drilled via holes.

13. The method claimed in claim 1, further comprising mounting a circuit component on the deposited dielectric layer.

14. The method claimed in claim 1, wherein the base substrate comprises a hermetic via, and

wherein one of the conductors is formed in contact the hermetic via.

15. The method claimed in claim 1, wherein the base substrate comprises a hermetic via, and wherein providing the base substrate comprises:

forming a via hole in the base substrate;

respectively forming multiple layers of conductive ink on sidewalls of the via hole;

filling a space between said sidewalls with conductive ink; and

sintering the conductive material in the via hole.

16. The method claimed in claim 15, wherein forming said multiple layers comprises:

introducing a conductive ink to the via hole;

applying a vacuum to the via hole to form a layer of said conductive ink on sidewalls of the hole; and

repeating said introducing and said applying to form said multiple layers of conductive ink on the sidewalls.

17. The method claimed in claim 16, wherein the conductive ink is introduced to the via hole by screen printing.

18. The method claimed in claim 16, wherein applying the vacuum eliminates voids in the conductive ink introduced into the via hole.

19. The method claimed in claim 16, wherein the vacuum is applied to one end of the via hole

20. The method claimed in claim 16, wherein the conductive ink used to fill the space between the sidewalls is less dilute than the conductive ink used to form said multiple layers.

21. The method claimed in claim 16, wherein applying the vacuum is followed by thermal processing to remove solvent and organic binder from the conductive ink.

22. The method claimed in claim 15, wherein providing the base substrate further comprises removing residual conductive material from surfaces of the base substrate.

23. The method claimed in claim 15, wherein the via hole is formed by laser drilling.

24. The method claimed in claim 23, wherein said laser drilling is followed by annealing to smooth the sidewalls of the via hole.

25. The method claimed in claim 1, wherein the base substrate comprises a hermetic via, and

wherein the method further comprises:

forming a conductor on the base substrate in contact with the hermetic via; and

forming a cap over the conductor and the hermetic via.

26. The method claimed in claim 25, wherein the cap is formed by a shadow mask deposition technique.

27. A multilayer circuit substrate, comprising:

a dielectric base substrate;

a conductor formed on the base substrate; and

a patterned vacuum deposited dielectric thin film formed on the base substrate and the conductor.

28. The structure claimed in claim 27, further comprising an electronic component mounted on the deposited dielectric thin film and electrically connected to the conductor through the deposited dielectric layer.

29. The structure claimed in claim 27, further comprising:

a second conductor formed on the deposited dielectric thin film and connected to the first conductor through the deposited dielectric thin film; and

a second patterned vacuum deposited dielectric thin film formed on the deposited dielectric layer and the second conductor.

30. The structure claimed in claim 29, further comprising an electronic component mounted on the second deposited dielectric thin film and electrically connected to the second conductor through the second deposited dielectric thin film.

31. The structure claimed in claim 27, wherein the base substrate comprises a hermetic via, and

wherein the conductor is formed in electrical contact with the hermetic via.